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IN THE CLAIMS:

1.   (currently amended) A method performed by a data processing system having a memory, comprising the steps of:

simulating an execution of an assignment statement of a hardware description language design specification in order to determine a logical value for a target signal of the assignment statement based upon a set of logical values for a set of input signals to the assignment statement;

identifying a subset of the input signals having an observably controllable effect on the logical value of the target signal based upon the logical values of the input signals and a functional interrelation of the input signals; and

determining a target tag value for the target signal comprising an identifier of the assignment statement and a history comprised of a first tag value of each for an input signal that is a member of the subset of input signals, wherein the first tag value includes an identifier of a first assignment statement temporally earlier than the assignment statement.

2.   (currently amended) The method of claim 1, wherein:

the step of identifying further comprises identifying a second subset of a set of input signals to a conditional statement of the hardware description language design specification having an observably controllable effect upon whether the assignment statement is simulated, membership in the second subset being based upon a logical value for each of an input signal to the conditional statement and a functional interrelation of the input signals to the conditional statement; and

the step of determining further comprises determining the history to be additionally comprised of a propagation of a tag value of [each]a signal of the second subset.

3.   (currently amended) The method of claim 1, wherein:

the step of identifying further comprises identifying a second subset of a set of input signals to a conditional expression of a conditional statement of the hardware description language design specification having an observably controllable effect upon whether the conditional expression is satisfied; and

the step of determining further comprises determining the history to be ~~additionally~~ comprised of a ~~propagation of a~~ tag value of [each]a̲ signal of the second subset.

4.   (currently amended) The method of claim 1, wherein ~~a propagation of a tag value to~~ the history is comprised of ~~creating~~ a copy of a̲[the] tag value of each input signal that is a member of the subset of input signals.

5.   (currently amended) The method of claim 2, wherein ~~a propagation of a tag value to~~ the history is comprised of ~~creating~~ a copy of a̲[the] tag value of each input signal that is a member of the subset of input signals.

6.   (currently amended) The method of claim 3, wherein ~~a propagation of a tag value to~~ the history is comprised of ~~creating~~ a copy of a̲[the] tag value of each input signal that is a member of the subset of input signals.

7.   (original) The method of claim 1, wherein:

the method further comprises the step of propagating the target tag value from the target signal, within a module instantiation comprising the assignment statement, to a higher-level signal of the hardware description language design specification.

8.   (original) The method of claim 7, wherein the step of propagating is performed in response to determining the logical value for the target signal.

9.   (original) The method of claim 7, wherein the target signal is defined as an output signal of the module instantiation.

10.   (original) The method of claim 7, wherein the propagation is performed by creating a copy of the target tag value.

11.   (original) The method of claim 1, wherein:
       the method further comprises the step of propagating the target tag value from the target signal, at a higher-level than a module instantiation of the hardware description language design specification, to a lower-level signal of the module instantiation.

12.   (original) The method of claim 11, wherein the step of propagating is performed in response to determining the logical value for the target signal.

13.   (original) The method of claim 11, wherein the lower-level signal is defined as an input signal of the module instantiation.

14.   (original) The method of claim 11, wherein the propagation is performed by creating a copy of the target tag value.

15.   (original) The method of claim 1, wherein observable controllability of a first input signal is determined by determining whether a flipping of a first logical value of the first input signal will cause a flipping of the logical value of the target signal.

16.   (original) The method of claim 1, wherein observable controllability of a first intermediate output signal of a first sub-function, wherein the functional interrelation of the input signals is comprised of the first sub-function, is determined by a rule-based consideration of the first sub-function and of a logical value for each input of the first sub-function.

17.   (original) The method of claim 16, wherein a logical value of the first sub-function is the same logical value assigned to the target signal.

18.   (original) The method of claim 16, wherein an input signal of the first sub-function is an input signal of the assignment statement.

19.   (original) The method of claim 1, wherein the target tag value is further comprised of a field for indicating a subsequent assignment statement that utilizes the target tag value.

20.   (currently amended) A data processing system having a memory, comprising the following:

a sub-system for simulating an execution of an assignment statement of a hardware description language design specification in order to determine a logical value for a target signal of the assignment statement based upon a set of logical values for a set of input signals to the assignment statement;

a sub-system for identifying a subset of the input signals having an observably controllable effect on the logical value of the target signal based upon the logical values of the input signals and a functional interrelation of the input signals; and

a sub-system for determining a target tag value for the target signal comprising an identifier of the assignment statement and a history comprised of a <u>first</u> tag value ~~of~~ ~~each~~ <u>for an</u> input signal that is a member of the subset of input signals<u>, wherein the first tag value includes an identifier of a first assignment statement temporally earlier than the assignment statement</u>.

21.   (currently amended) A computer program product comprising:

a computer usable medium having computer readable code embodied therein;

computer readable program code devices configured to cause a computer to effect simulating an execution of an assignment statement of a hardware description language design specification in order to determine a logical value for a target signal of

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the assignment statement based upon a set of logical values for a set of input signals to the assignment statement;

computer readable program code devices configured to cause a computer to effect identifying a subset of the input signals having an observably controllable effect on the logical value of the target signal based upon the logical values of the input signals and a functional interrelation of the input signals; and

computer readable program code devices configured to cause a computer to effect determining a target tag value for the target signal comprising an identifier of the assignment statement and a history comprised of a <u>first</u> tag value ~~of each~~ <u>for an</u> input signal that is a member of the subset of input signals<u>, wherein the first tag value includes an identifier of a first assignment statement temporally earlier than the assignment statement</u>.